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EXAMINER	
ZALEPA, GEORGE D	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,025	SHIPPY, DAVID	
	Examiner	Art Unit	
	George D. Zalepa	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been considered by the examiner.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Architected register file system utilizes status and control registers to control read/write operations between concurrently executing threads.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 10-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Furthermore, the computer program of claims 10-12 is not tangibly embodied on a computer-readable medium. As written, the computer program can be embodied on a non-statutory element such as a carrier wave or piece of paper.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5, 7-8 rejected under 35 U.S.C. 102(b) as being anticipated by Sollars (US Pat. No. 5,900,025).

6. Regarding **independent claim 1,**

7. Sollars discloses *an architected register file system at least configured to utilize a plurality of threads, comprising: a plurality of register files* [see Sollars, Col. 5, lines 21-30], *wherein each register file of the plurality of register files at least corresponds to at least one thread of the plurality of threads* [see Sollars, Col. 5, lines 24-30; Examiner's note: In this cite, Sollars discloses a multi-dimensional register file which would allow for multiple threads to occupy a register file in a subset dimension. This idea is illustrated in Fig. 2a of US Pat. No. 6,081,880 (to Sollars as well) incorporated by reference by Sollars in '025]*; a plurality of Status and Control Registers (SCR)* [see Sollars, Fig. 1, element 20a; Col. 5, lines 31-34], *wherein each SCR corresponds to at least one register file of the plurality of register files* [see Sollars, Col. 2, lines 2-6]*; and a plurality of control bit sets, wherein each control bit set corresponds to at least one SCR* [see Sollars, Fig. 5; Examiner's note: Fig. 5 illustrates an SCR containing control bit sets.], *and wherein each control bit set is at least configured to allow a thread associated with an associated SCR to utilize other register files associated with other threads* [see Sollars, Col. 15, lines 60-66].

8. Regarding **claim 2**,

9. Sollars discloses *the architected register file system of claim 1, wherein the architected register file system further comprises a decoder, wherein the decoder at least determines desired operations for an instruction* [see Sollars, Col. 2, line 64 to Col. 3, line 1; Examiner's note: It is inherent that the function of a decoder is to determine the operations requested of an instruction.].

10. Regarding **claim 3**,

11. Sollars discloses *the architected register file system of claim 1, wherein plurality of control bits further comprise a plurality of bit doublets* [see Sollars, Fig. 9A, elements "sl" and "ll"], *wherein a first bit of a bit doublet corresponds to a read function* [see Sollars, Col. 10, lines 57-62, "...of a load operation is to be locked..."], *and wherein a second bit of the bit doublet corresponds to a write function* [see Sollars, Col. 10, lines 51-57, "...of a store operation is to be locked..."].

12. Regarding **claim 4**,

13. Sollars discloses *the architected register file system of claim 3, wherein the architected register file system further comprises: an address control, wherein the address control at least determines addresses with the plurality of register files* [see Sollars, Col. 5, lines 24-30; Examiner's note: Sollars incorporates US Pat. No. 6,081,880 (to Sollars), which discloses the operation of the operand, register file (Sollars ('025), Fig. 2, element 22a). In Figure 2a of '880, Sollars shows a multidimensional register file wherein element 22' is used to address register files 22a-*. Therefore, by reference, Sollars shows an address control that determines the address of a plurality of register files.]*; and at least one execution unit* [see Sollars, Fig. 2, element 14], *wherein the execution is at least configured to perform the operations of a input instruction within the plurality of register files* [see Sollars, Col. 6, lines 24-34].

14. Regarding **claim 5**,

15. Sollars discloses *the architected register file system of claim 3, wherein the plurality of bit doublets further comprises that each bit doubled at least corresponds to enabling the use of at least one register file associated with another thread* [see Sollars, Col. 10, lines 51-62 (enabling writing and reading to/from a register file); Col. 15, lines 60-66 (accessing other multiple threads)].

16. Regarding **independent claim 7**,

17. Sollars discloses *a method for utilizing a plurality of register files* [see Sollars, Col. 5, lines 21-30] *with associated SCRs in a multithread system* [see Sollars, Fig. 1, element 20a; Col. 5, lines 31-34], *wherein each register file is at least associated with one thread of a plurality of threads* [see Sollars, Col. 5, lines 24-30; Examiner's note: In this cite, Sollars discloses a multi-dimensional register file which would allow for multiple threads to occupy a register file in a subset dimension. This idea is illustrated in Fig. 2a of US Pat. No. 6,081,880 (to Sollars as well) incorporated by reference by Sollars in '025], *comprising: receiving an instruction for a first thread of the plurality of threads* [see Sollars, Col. 2, line 64 to Col. 3, line 1, "...fetching...instructions for the active threads..."], *wherein the first thread is at*

least associated with a first SCR [see Sollars, Col. 2, lines 2-6; Examiner's note: Since the SCR is associated with a threads register file, it is inherently associated with the thread.]; *decoding the instruction to at least determine performance operations* [see Sollars, Col. 2, line 64 to Col. 3, line 1, "...decoding...instructions for the active threads..."]; *determining if the first thread is enabled to at least utilize register files associated with other threads* [see Sollars, Col. 10, lines 57-62]; *and executing the instruction, wherein the step of executing at least utilizes whatever register files that are enabled* [see Sollars, Col. 15, lines 60-66].

18. Regarding **claim 8**,

19. Sollars discloses *the method of claim 7, wherein the step of determining if the first thread is enabled, further comprises measuring logical levels of control bits associated with the first SCR, wherein the control bits comprise a plurality of bit doublets* [see Sollars, Fig. 9A, elements "sl" and "ll"], *and wherein each bit doubled at least corresponds to enabling the use of at least one register file associated with another thread* [see Sollars, Col. 10, lines 51-62; Col. 15, lines 60-66].

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sollars.

22. Regarding **claim 6**,

23. Sollars discloses the limitations as stated in **claim 5**.

24. Sollars also discloses *one bit* [of a doublet] *is at least configured to correspond to a read function* [see Sollars, Col. 10, lines 57-62, "...of a load operation is to be locked..."] and *one bit* [of a doublet] *is*

at least configure to correspond to a write function [see Sollars, Col. 10, lines 51-57, "...of a store operation is to be locked..."].

25. Sollars does not explicitly disclose *a logic high or '1'* enabling *the first thread to read from another register file* or *a logic high or '1'* enabling *the first thread to write to another register file.*

26. However, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a logic high value to correspond to the enablement of a value stored within a register. At the time of invention, the use of a logic high signal as an indication of an enabled function would have been common knowledge, such as the concept of register flags indicating certain conditions. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a active-high scheme to enable access to a register file.

27. Regarding **claim 9**,

28. Sollars discloses the limitations as stated in **claim 8**.

29. Sollars does not explicitly disclose *determining if any bits are `1` or logic high, wherein the `1` or the logic high enables the first thread to read or write to another register file.*

30. However, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a logic high value to correspond to the enablement of a value stored within a register. At the time of invention, the use of a logic high signal as an indication of an enabled function would have been common knowledge, such as the concept of register flags indicating certain conditions. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a active-high scheme to enable access to a register file.

31. Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sollars in view of Tanenbaum (Andrew S. Tanenbaum. Structured Computer Organization, 1984. Pg. 10-11; herein referred to as "Tanenbaum").

32. Regarding **independent claim 10**,

33. Sollars discloses *receiving an instruction for a first thread of the plurality of threads* [see Sollars, Col. 2, line 64 to Col. 3, line 1, "...fetching...instructions for the active threads..."], *wherein the first thread is at least associated with a first SCR* [see Sollars, Col. 2, lines 2-6; Examiner's note: Since the SCR is associated with a threads register file, it is inherently associated with the thread.]...*decoding the instruction to at least determine performance operations* [see Sollars, Col. 2, line 64 to Col. 3, line 1, "...decoding...instructions for the active threads..."];...*determining if the first thread is enabled to at least utilize register files associated with other threads* [see Sollars, Col. 10, lines 57-62]; *and...executing the instruction, wherein the step of executing at least utilizes whatever register files that are enabled* [see Sollars, Col. 15, lines 60-66].

34. Sollars does not disclose the above method being performed by a computer program product.

35. However, Tanenbaum discloses that "hardware and software are logically equivalent" and that any hardware apparatus can be simulated in software [see Tanenbaum, p. 11, lines 11-13]. The advantage of implementing the method disclosed within claim 18 within a machine-accessible medium would have been to exploit the advantages of software-based approaches such as cost or ease of upgrading [see Tanenbaum, p. 11, lines 13-15]. This advantage would have motivated one of ordinary skill in the art to implement the method disclosed in the body of claim 10 in software as opposed to in hardware.

36. Regarding **claim 11**,

37. Sollars and Tanenbaum disclose the limitations as stated in **independent claim 10**.

38. Sollars further discloses *measuring logical levels of control bits associated with the first SCR, wherein the control bits comprise a plurality of bit doublets* [see Sollars, Fig. 9A, elements "sl" and "ll"], *and wherein each bit doubled at least corresponds to enabling the use of at least one register file associated with another thread* [see Sollars, Col. 10, lines 51-62; Col. 15, lines 60-66].

39. Regarding **claim 12,**

40. Sollars and Tanenbaum disclose the limitations as stated in **claim 11**.

41. Sollars does not explicitly disclose *determining if any bits are `1` or logic high, wherein the `1` or the logic high enables the first thread to read or write to another register file.*

42. However, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a logic high value to correspond to the enablement of a value stored within a register. At the time of invention, the use of a logic high signal as an indication of an enabled function would have been common knowledge, such as the concept of register flags indicating certain conditions. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a active-high scheme to enable access to a register file.

43. Regarding **independent claim 13,**

44. Sollars discloses *a processor for utilizing a plurality of register files* [see Sollars, Col. 5, lines 21-30] *with associated SCRs in a multithread system* [see Sollars, Fig. 1, element 20a; Col. 5, lines 31-34], *wherein each register file is at least associated with one thread of a plurality of threads* [see Sollars, Col. 5, lines 24-30; Examiner's note: In this cite, Sollars discloses a multi-dimensional register file which would allow for multiple threads to occupy a register file in a subset dimension. This idea is illustrated in Fig. 2a of US Pat. No. 6,081,880 (to Sollars as well) incorporated by reference by Sollars in '025].

45. Sollars also discloses *receiving an instruction for a first thread of the plurality of threads* [see Sollars, Col. 2, line 64 to Col. 3, line 1, "...fetching...instructions for the active threads..."], *wherein the first thread is at least associated with a first SCR* [see Sollars, Col. 2, lines 2-6; Examiner's note: Since the SCR is associated with a threads register file, it is inherently associated with the thread.]...*decoding the instruction to at least determine performance operations* [see Sollars, Col. 2, line 64 to Col. 3, line 1, "...decoding...instructions for the active threads..."]; ...*determining if the first thread is enabled to at least utilize register files associated with other threads* [see Sollars, Col. 10, lines 57-62]; *and...executing*

the instruction, wherein the step of executing at least utilizes whatever register files that are enabled [see Sollars, Col. 15, lines 60-66].

46. Sollars does not disclose the above method being performed by a computer program within a processor.

47. However, Tanenbaum discloses that "hardware and software are logically equivalent" and that any hardware apparatus can be simulated in software [see Tanenbaum, p. 11, lines 11-13]. The advantage of implementing the method disclosed within claim 18 within a machine-accessible medium would have been to exploit the advantages of software-based approaches such as cost or ease of upgrading [see Tanenbaum, p. 11, lines 13-15]. This advantage would have motivated one of ordinary skill in the art to implement the method disclosed in the body of claim 10 in software as opposed to in hardware.

48. Regarding **claim 14**,

49. Sollars and Tanenbaum disclose the limitations as stated in **independent claim 13**.

50. Sollars further discloses *measuring logical levels of control bits associated with the first SCR, wherein the control bits comprise a plurality of bit doublets* [see Sollars, Fig. 9A, elements "sl" and "ll"], *and wherein each bit doubled at least corresponds to enabling the use of at least one register file associated with another thread* [see Sollars, Col. 10, lines 51-62; Col. 15, lines 60-66].

51. Regarding **claim 15**,

52. Sollars and Tanenbaum disclose the limitations as stated in **claim 14**.

53. Sollars does not explicitly disclose *determining if any bits are `1` or logic high, wherein the `1` or the logic high enables the first thread to read or write to another register file.*

54. However, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a logic high value to correspond to the enablement of a value stored within a register. At the time of invention, the use of a logic high signal as an indication of an enabled function would have been

common knowledge, such as the concept of register flags indicating certain conditions. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to utilize a active-high scheme to enable access to a register file.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Zalepa whose telephone number is (571) 272-6754. The examiner can normally be reached on Monday-Friday (alt. Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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